DAC Correction Filter
AH1002-DCF

Product Description AH1002DS V1.0 Nov., 2013

INTRODUCTION

The AH1002-DCF DAC Correction Filter (DCF) FPGA core family provides correction in the discrete-time digital domain for the sin(x)/x frequency response of a typical Digital to Analog Converter (DAC). Anchor Hill's DCF cores are implemented as multiplierless Finite Impulse Response (FIR) filters with configurable input and output bit widths and automatic arithmetic saturation of the output to prevent numeric rollover distortion.

FEATURES

- Efficient, multiplier-free design minimizes resource utilization and power consumption
- Configurable input and output widths
- Multiple tap-length configurations including 9-tap, 7-tap, and 5-tap
- Arithmetic overflow output monitor
- Clock enable
- Output saturation prevents arithmetic rollover
- Static resettable output
- Registered input, registered output
- Clock rates over 714 MHz supported
- Includes complete simulation and verification software support suite
- Custom designs and configurations available

DESCRIPTION

In sampled systems the DACs used for signal conversion from digital to analog nearly universally include a zero-order hold function of the output analog signal as part of the conversion process. The zero-order hold unavoidably applies a sin(x)/x frequency response to the output signal with the first null at the conversion sample rate frequency. The sin(x)/x response of the zero-order hold can be accurately corrected by applying a compensating x/sin(x) response. The AH1002-DCF filter family produces the required compensating response so that the frequency

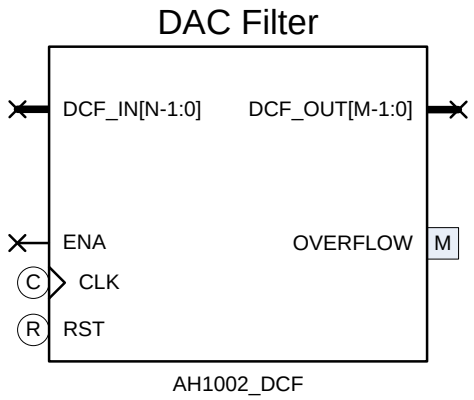

Figure 1. DAC Correction Filter Schematic Symbol

spectrum amplitude of the converted signal is accurately reproduced up to approximately 0.4 times the sampling frequency or higher.

The AH1002-DCF filter responses are shown in Figure 3 compared to an ideal x/sin(x) response. The unity gain point for each filter is normalized to occur near f = 0.25 rad/sample, that is, with the sampling frequency defined as f_s = 1.0. Generally there is a tradeoff between filter complexity and accuracy, and in this case it can be seen in Fig. 3 that the 9-tap version's response maintains proximity to the ideal response at higher frequencies. The low-frequency response of the filters is shown in Figure 4, where it can be seen that the 5-tap filter deviates from the ideal response less than 0.1dB.

The implementation complexity of the filters is kept low using Anchor Hill's proprietary design techniques that provide both high accuracy and high implementation efficiency. Multiplier resources are often strained in FPGA designs and the AH1002-DCF filters use no multipliers in order to preserve limited FPGA resources like Xilinx DSP48. Resource utilization for Xilinx targets is shown in Tables 2a - 2c. Filter gain and latency are shown in Table 3.

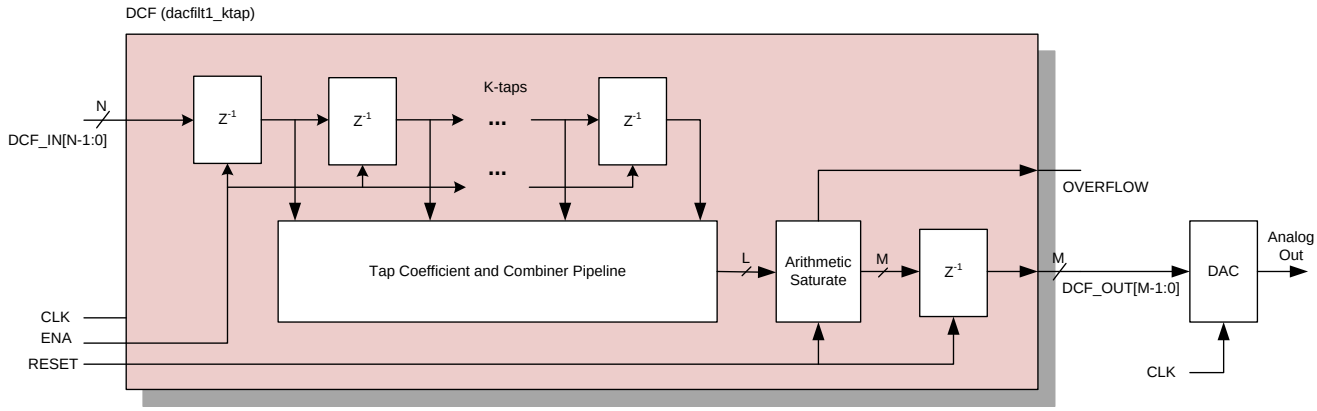

Figure 2. AH1002-DCF DAC Correction Filter block diagram showing integration with a typical Digital to Analog Converter.

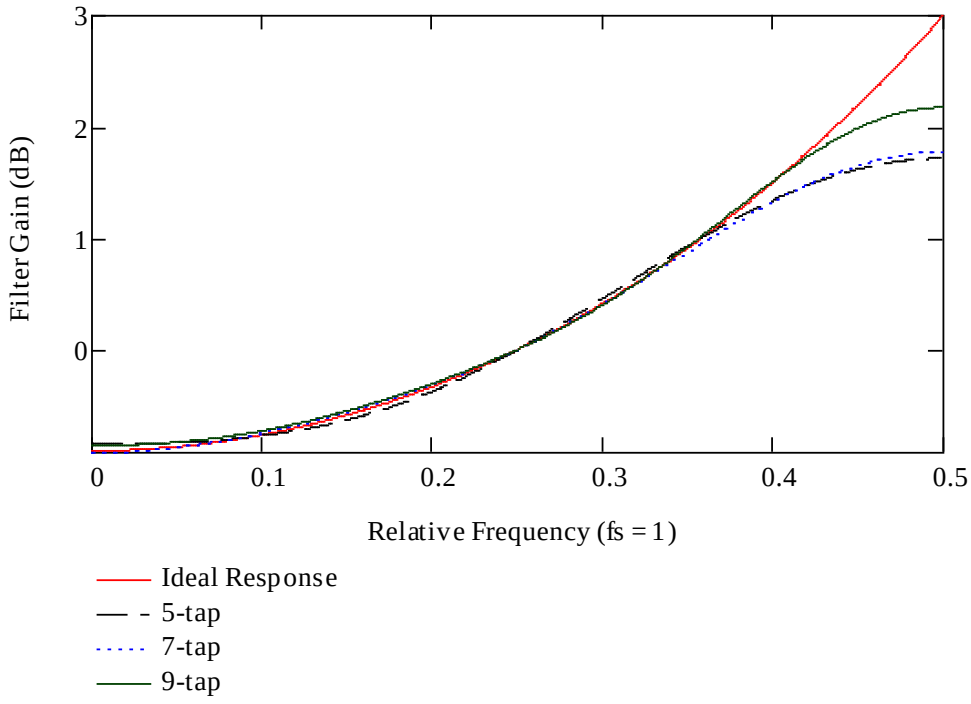

Figure 3. Ideal x/sin(x) and Implemented frequency response for the AH1002-DCF DAC Correction Filters

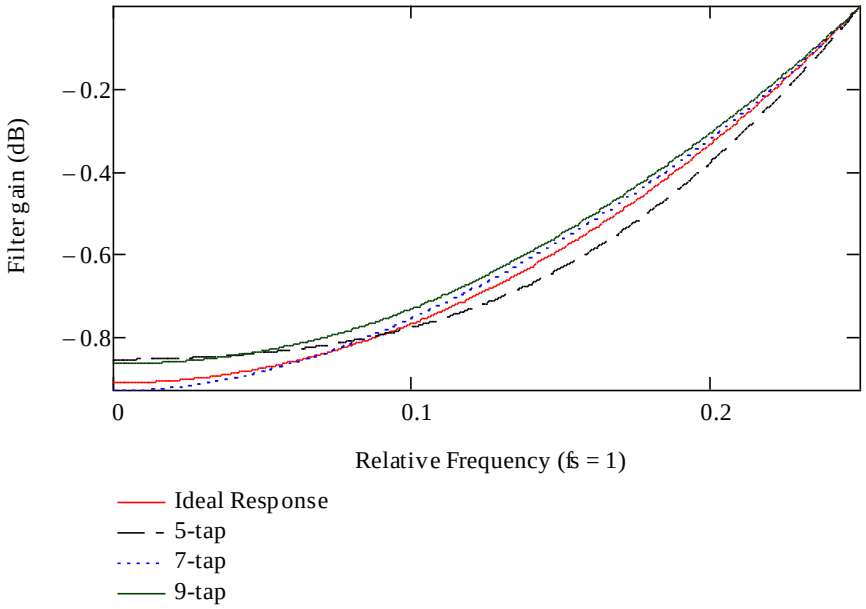

Figure 4. Close-up view of Ideal x/sin(x) and Implemented AH1002-DCF frequency response.

SIGNAL DESCRIPTIONS

Signal	Direction	Description
DCF_IN[N-1:0]	Input bus	Filter input signal
ENA	Input	Input clock enable
CLK	Input	System clock input
RST	Input	Module reset
DCF_OUT[M-1:0]	Output bus	Filter output signal
OVERFLOW	Output	Active if arithmetic overflow in output

Table 1. DAC Correction Filter Input and Output Signal Descriptions

Inputs

DCF_IN[N:0] - This is the filter input signal bus. The signal is internally registered and represented in two's complement signed binary format. The input signal bus width is parameterized.

ENA - This is the input clock enable for the filter. When **ENA** is asserted (high) the **DCF_IN** input and input tap delay line are clocked at the rising edge of **CLK**. **ENA** can be permanently asserted, that is tied high, in order for the filter to process input samples every clock cycle. Figure 5 shows **ENA** timing.

CLK - System clock input.

RST - Reset. The internal logic is forced to an initialization state when asserted. The **DCF_OUT** and **OVERFLOW** signals are set to zero when asserted. The tap pipeline and combining pipelines are not affected by **RST**.

Outputs

DCF_OUT[M:0] - Two's complement filter output. The output width is parameterized.

OVERFLOW - Arithmetic overflow indicator for the filter output. The **DCF_OUT** output is processed by an arithmetic saturation stage when taken from the tap combiner. If the filter output cannot be represented by the **DCF_OUT** output precision, the output is set to the Full Scale value with the same sign and **OVERFLOW** is set until the next output sample.

Resource Utilization and Speed

The DAC Correction Filter has been synthesized with the resource utilizations and speeds shown in Table 2 for the indicated Xilinx device families. Results shown are from the Xilinx XST synthesis tools with trimming disabled and the specific devices selected as indicated. Speeds shown are for -2 parts.

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	Max Freq (MHz)
Kintex-7	xc7k70t	178	135	41	144	0	707
Spartan-6	xc6slx75t	179	140	43	151	0	350
Virtex-5	Xc5vlx50t	178	117	51	181	0	510
Virtex-6	xc6vlx75t	179	134	41	147	0	647

Table 2a. DACfilt1_5tap Resource Utilization for certain Xilinx Device Families

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	Max Freq (MHz)
Kintex-7	xc7k70t	214	172	50	181	0	714
Spartan-6	xc6slx75t	214	170	55	197	0	410
Virtex-5	Xc5vlx50t	214	154	63	218	0	516
Virtex-6	xc6vlx75t	214	168	51	185	0	547

Table 2b. DACfilt1_7tap Resource Utilization for certain Xilinx Device Families

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	Max Freq (MHz)
Kintex-7	xc7k70t	308	235	73	260	0	714
Spartan-6	xc6slx75t	308	245	75	264	0	410
Virtex-5	Xc5vlx50t	309	214	87	314	0	516
Virtex-6	xc6vlx75t	308	224	82	281	0	654

Table 2c. DACfilt1_9tap Resource Utilization for certain Xilinx Device Families

Input and Output Timing

The input and output timing is shown in Fig. 4 below. ENA can be asserted constantly in order to update input and output samples every clock cycle.

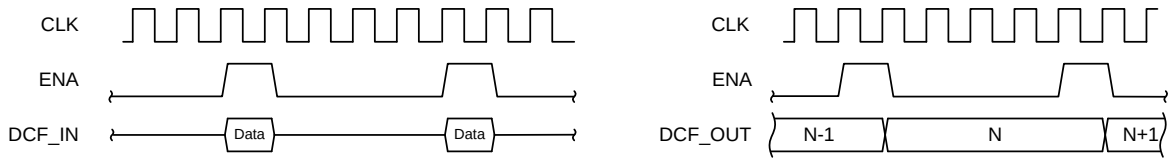

Figure 5. Timing diagrams for the signal input path (left) and output path (right).

DCF Version	DC Gain (linear)	Gain at $f_s/4$ (linear)	Filter latency (clock cycles)
9 tap	0.895	0.988	12
7 tap	0.898	1.0	10
5 tap	0.906	1.0	8

Table 3. Gains and latencies for the standard AH1002-DCF filters.

Ordering and Delivery

The AH1002-DCF core is supplied as a Xilinx ngc or EDIF netlist for a user-specified Xilinx device. Each license is a permanent site license that is device-locked to the specified target device. Unlimited instantiations in the specified target device are allowed under the terms of the license. A port to or instantiation in a different device requires a new license from Anchor Hill. Each license includes six months of technical support from Anchor Hill.

Each license also includes Verilog verification test bench suites to provide a design validation and test development platform for integrators. Some test suites also include supporting C-language and/or Matlab/Octave programs to provide test stimulus files and output analysis tools.

Certain customizations, such as changing the number of taps, latency, frequency response, or the input or output precision, are available. Source code is also available. Contact Anchor Hill Communications for more information.

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