Mobile Phase Recovering Equalizer AH1000-MPRE

Product Description AH1000DS V1.2 May, 2014

INTRODUCTION

The Mobile Phase Recovering Equalizer (MPRE) FPGA core combines Channel Equalization, Phase Recovery, and Symbol Slicing in a single module. Advanced, patented signal processing in the MPRE provides robust and reliable QPSK demodulation in high Doppler and mobile multipath environments. Mobile multipath radio environments that are too harsh for broadband single-carrier QPSK reception can be used reliably with the MPRE.

FEATURES

- 17-tap complex-arithmetic LMS Channel Equalizer with adaptation bandwidth and leakage rate control as well as independent coefficient hold and reset controls
- VV4 Viterbi-Viterbi algorithm for signal phase recovery and differential detection
- Integrated Symbol Slicer provides demodulated soft-decision outputs
- AGC output controls in proportional and up/dn format for constant-modulus and phase-locked processing
- Phase-locked constellation output
- Equalized signal output for FLL or other processing
- Clock rates up to 200 MHz supported
- Symbol rates up to 1/5 of clock rate

DESCRIPTION

For mobile systems the presence of multipath reflections and Doppler-induced frequency offsets can create a challenge for demodulation of broadband single-carrier PSK signals. Spatial nulls created by destructive multipath interference are characterized by a signal phase reversal across the null, so traversing a null typically results in loss of phase lock in a traditional single-carrier receiver. Since spatial nulls cannot be avoided in mobile applications these loss-of-synchronization events result in unacceptable performance for broadband

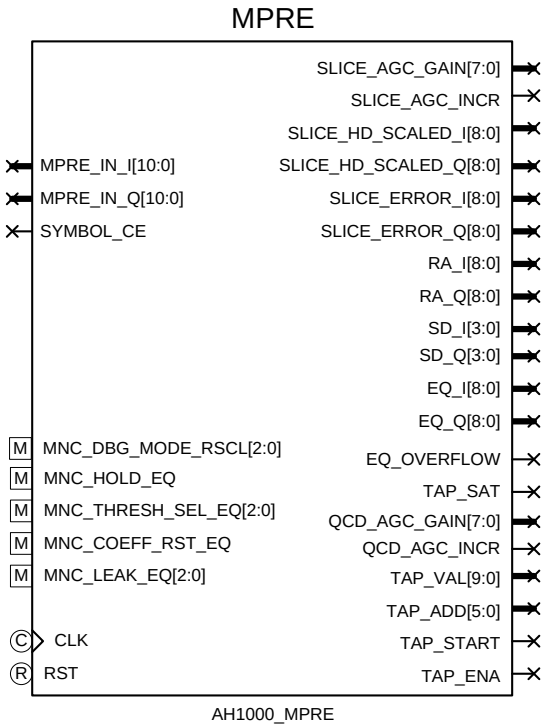

Figure 1. MPRE Schematic Symbol

systems. The MPRE solves this problem by using a Viterbi-Viterbi [1] feed-forward phase synchronization algorithm that averages the phase over the most recent symbols. This provides substantial robustness by ignoring phase perturbations that would otherwise be outside the bandwidth of a phase-recovery PLL and results in a fraction of one dB loss in performance in AWGN (see Figure 3).

For symbol rates higher than around a hundred kiloHertz or so, multipath reflections will result in non-flat fading which requires a Channel Equalizer to mitigate. Training an equalizer that will provide good performance tradeoffs, like the LMS system used in the MPRE, requires error feedback from the demodulated signal that is not available in a non-coherent system. The MPRE uses a patented technique to accurately train the equalizer using an innovative feedback arrangement between the VV4 Phase Synchronizer and Equalizer.

APPLICATION

The MPRE is ideal for medium-to-high data rate applications when range, power efficiency and reliability in mobile channels are desired. The MPRE uses single-carrier QPSK modulation which allows the use of low Peak-to-Average-Power-Ratio (PAPR) signaling to provide both longer range and prolonged battery life. The MPRE's Channel Equalizer can effectively mitigate typical multipath channel delay spreads encountered using omni-directional antennas at symbol rates approaching six to eight Megahertz.

Symbol Rate	Data Rate (R = 1/2-7/8)	EQ Length (uSec)
500 kHz	500-875 kbps	34 us
1 MHz	1-1.75 Mbps	17 us
1.5 MHz	1.5-2.625 Mbps	11.333 us
2 MHz	2-3.5 Mbps	8.5 us
5 MHz	5-8.75 Mbps	3.4 us
6 MHz	6-10.5 Mbps	2.833 us
8 MHz	8-14 Mbps	2.125 us

Table 1. Effective Equalizer Length

Table 1 shows the effective length of the MPRE's 17-tap Channel Equalizer as a function of QPSK symbol rate and corresponding data rates for FEC code rates of R = 1/2 to R = 7/8. For symbol rates above six to eight Megahertz directional antennas can be used to reduce the channel delay spread and increase the potential data rates for mobile data transmission.

The MPRE fits easily into the signal flow of most single-carrier demodulators with a minimal amount of configuration and supporting input signals. Figure 2 shows a block diagram of a typical demodulator with the MPRE installed in the signal flow chain. With only the time-synchronized symbols as input, the MPRE provides:

- Equalized symbols to feed a Frequency-Locked Loop or other processing elements
- Phase-locked, derotated constellation symbols
- Differentially detected soft-decision outputs for FEC decoding
- Sliced symbol error vectors to facilitate SNR estimation
- AGC control signals

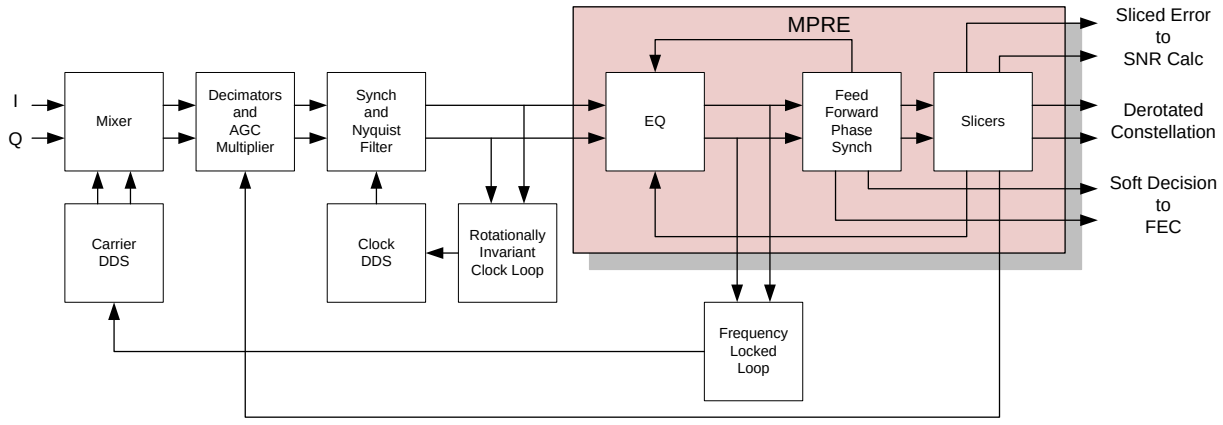

Figure 2. Signal flow diagram showing how the MPRE integrates easily into a typical demodulator.

PERFORMANCE

The MPRE necessarily uses differential detection in order to maintain robustness against the phase perturbations typically encountered in mobile channels. A consequence of this is that there is a slight performance loss compared to a traditional fully-coherent QPSK system that might be used in a fixed-link system. The feed-forward Viterbi-Viterbi phase synchronization processing used in the MPRE minimizes this performance loss while achieving greatly improved reliability in mobile channels. Figure 3 shows the Bit Error Rate (BER) performance of the MPRE in AWGN compared to uncoded fully coherent, coherent differentially encoded, and differentially detected signals. Also shown is the BER performance of the MPRE using a convolutional code with R = 1/2 and k = 7 compared to a typical coherent system using the same code. The advanced signal processing within the MPRE maintains performance within less than 1 dB of a differentially-encoded coherent system with far greater immunity to the perturbations of a mobile channel. This provides significant range extension compared to multi-carrier systems with higher PAPR.

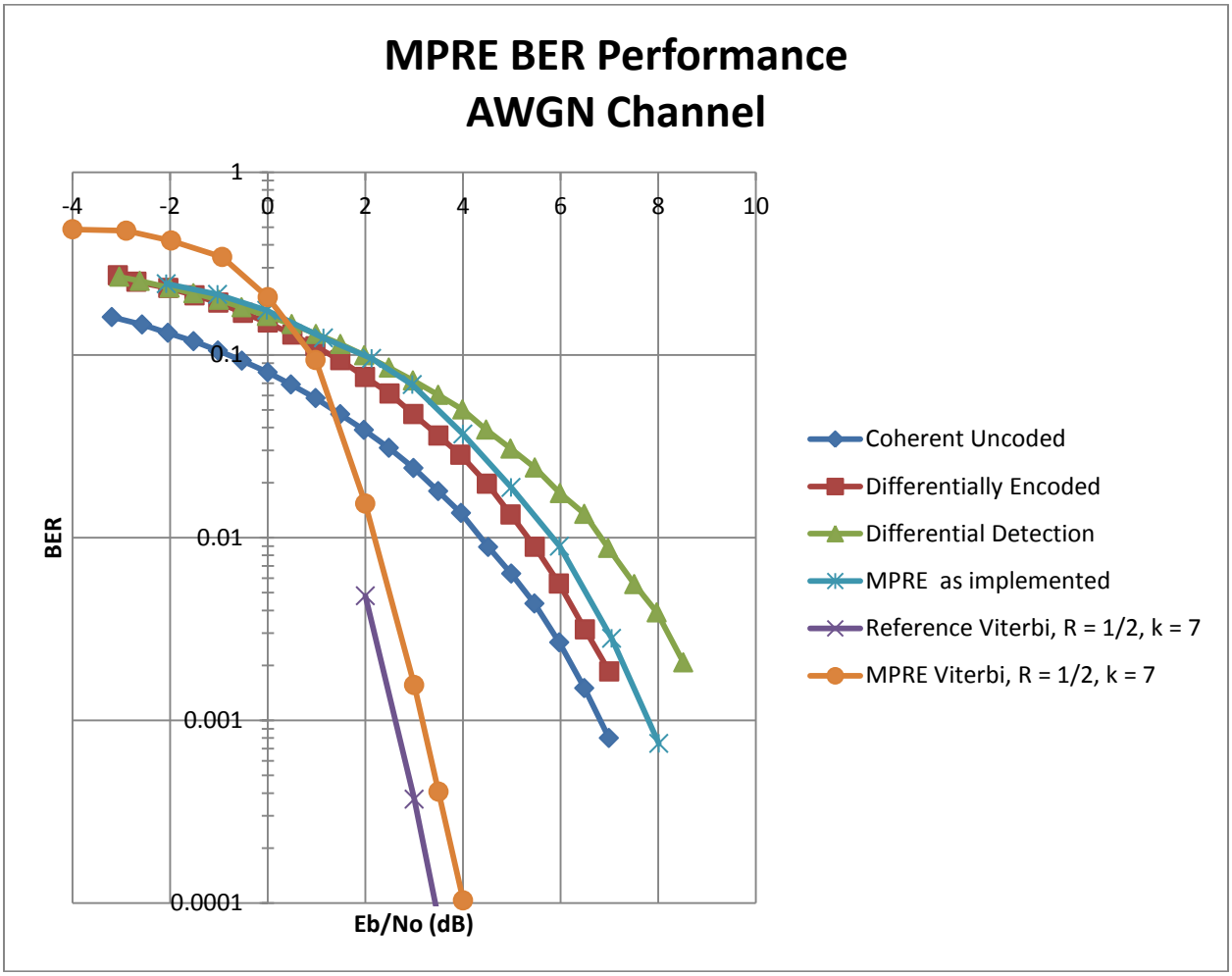

Figure 3. BER Performance of the MPRE in AWGN for both coded and uncoded cases. The MPRE generally operates within less than 1dB of a differentially-encoded coherent system.

SIGNAL DESCRIPTIONS

Signal	Direction	Description
MPRE_IN_I/Q[10:0]	Input bus	Baseband signal input
SYMBOL_CE	Input	Symbol input clock enable
CLK	Input	System clock input
RST	Input	Module reset
MNC_DBG_MODE_RSCL[2:0]	Input bus	Reserved - Set to zero
MNC_HOLD_EQ	Input	Equalizer coefficient hold
MNC_THRESH_EQ_SEL[2:0]	Input bus	Equalizer adaptation bandwidth (mu)
MNC_COEFF_RST_EQ	Input	Equalizer coefficient reset
MNC_LEAK_EQ[2:0]	Input bus	Equalizer coefficient leak rate (0 = no leak)
SLICE_AGC_GAIN[7:0]	Output	Slicer proportional AGC control (sliced constellation style)
SLICE_AGC_INCR	Output	Slicer AGC up/down control (sliced constellation style)
SLICE_HD_SCALED_I/Q[8:0]	Output bus	Hard-Decision output scaled to constellation signal space
SLICE_ERROR_I/Q[8:0]	Output bus	Sliced error vector - useful for noise power estimation
RA_I/Q[8:0]	Output bus	Derotated, phase-locked constellation
SD_I/Q[8:0]	Output bus	Differentially detected Soft Decision output
EQ_I/Q[8:0]	Output bus	Equalizer output
EQ_OVERFLOW	Output	Active if arithmetic overflow in any Equalizer tap
TAP_SAT	Output	Active if any Equalizer tap coefficient reaches max value
QCD_AGC_GAIN[7:0]	Output bus	QCD proportional AGC control (constant modulus style)
QCD_AGC_INCR	Output	QCD AGC up/down control (constant modulus style)
TAP_VAL[9:0]	Output bus	Equalizer tap debug coefficient value readout
TAP_ADD[5:0]	Output bus	Equalizer tap debug coefficient address readout
TAP_START	Output	Equalizer tap debug readout cycle start indicator
TAP_ENA	Output	Equalizer tap debug readout output enable

Table 2. MPRE Input and Output Signal Descriptions

Inputs

MPRE_IN_I/Q[10:0] - These are the I and Q baseband, time-synchronized, symbol inputs represented in two's complement. The default input width is eleven bits but is parameterized.

SYMBOL_CE - This is the input clock enable for the MPRE_IN_I/Q input signals. When SYMBOL_CE is asserted (high) the MPRE_IN_I and MPRE_IN_Q inputs are clocked in at the rising edge of CLK. SYMBOL_CE should not be asserted longer than one period of CLK and should remain inactive for at least four clock periods after assertion. The MPRE output signals are also updated when SYMBOL_CE is active.

CLK - System clock input.

RST - Reset. The internal logic is forced to an initialization state when asserted.

MNC_DBG_MODE_RSCL[2:0] - This is a reserved debug input and should be set to zero.

MNC_HOLD_EQ - When asserted the equalizer stops adapting and freezes the tap coefficients.

MNC_THRESH_EQ_SEL[2:0] - This three-bit value controls the adaptation bandwidth, or step size, (mu) of the Equalizer adaptation. Eight discrete power-of-two selections are used such that larger values result in wider adaptation bandwidth, which scales with the symbol rate, Rs.

000 : 4.4545e-05 * Rs (narrowest adaptation BW)
001 : 8.5580e-05 * Rs
010 : 1.7132e-04 * Rs
011 : 3.4941e-04 * Rs
100 : 6.9735e-04 * Rs
101 : 1.3889e-03 * Rs
110 : 2.7548e-03 * Rs
111 : 6.2893e-03 * Rs (widest adaptation BW)

MNC_COEFF_RST_EQ - Equalizer Coefficient Reset. When asserted (high) the Equalizer coefficients are set to zero.

MNC_LEAK_EQ[2:0] - Equalizer tap coefficient leakage control. Coefficients will slowly decay to zero in the absence of significant error feedback when this feature is enabled. Set MNC_LEAK_EQ = 0 to disable coefficient leakage. The leak rate increases by 4x for each increment towards 7.

Outputs

SLICE_AGC_GAIN[7:0] - Unsigned proportional gain control signal. Updated once per symbol. This is the eight MSBs of a twelve-bit counter that increments or decrements once each symbol depending on whether the current sliced symbol is within the AGC slice boundary or not. The demanded gain is proportional to the output value, such that an input signal that is too small will result in SLICE_AGC_GAIN increasing. See the section below regarding AGC Control for more information.

SLICE_AGC_INCR - Up/Down AGC control signal. Updated once per symbol. This is the increment/decrement control signal for the counter that drives the SLICE_AGC_GAIN output. When active (high) the counter is incremented, else it is decremented. See the section below regarding AGC Control for more information.

SLICE_HD_SCALED_I/Q[8:0] - Hard-decision output scaled to represent a two's complement ideal received constellation. This can be used as the reference signal for an external SNR estimator.

SLICE_ERROR_I/Q[8:0] - The two's complement sliced error vector or the vector difference between the ideal estimated received constellation, SLICE_HD_SCALED_I/Q, and the received symbol vector, RA_I/Q. This can be used as the signal noise component in an external SNR estimator.

RA_I/Q[8:0] - Two's complement, phase-locked, derotated constellation output.

SD_I/Q[8:0] - Demodulated soft-decision output.

EQ_I/Q[8:0] - Two's complement Equalizer output. This signal is not phase-locked and can be used at the input to a Frequency Locked Loop (FLL) or other baseband processing elements.

EQ_OVERFLOW - Arithmetic overflow indicator for the Equalizer outputs. The EQ_I/Q outputs are processed by a Clip-and-Round stage when taken from the tap accumulators. If the output is saturated EQ_OVERFLOW is set until the next output symbol.

TAP_SAT - Saturation indicator for the Equalizer coefficients. If any coefficient reaches its maximum or minimum value this signal will assert until the condition clears.

QCD_AGC_GAIN[7:0] - Unsigned proportional gain control signal. Updated once per symbol. This is the eight MSBs of a twelve-bit counter that increments or decrements once each symbol depending on whether the current Equalizer output symbol magnitude is within the AGC slice boundary or not. The demanded gain is proportional to the output value, such that an input signal that is too small will result in QCD_AGC_GAIN increasing. See the section below regarding AGC Control for more information.

QCD_AGC_INCR - Up/Down AGC control signal. Updated once per symbol. This is the increment/decrement control signal for the counter that drives the QCD_AGC_GAIN output. When active (high) the counter is incremented, else it is decremented. See the section below regarding AGC Control for more information.

TAP_VAL[9:0] - Two's complement Equalizer tap coefficient values, automatically read out as the equalizer processes symbols.

TAP_ADD[5:0] - The address of the tap coefficient currently being read out. The address starts at 0 for the I-channel coefficient of Tap G (the 17th tap), followed by the I-to-Q cross tap at address 1, the Q-to-I cross tap at address 2, and the Q-channel coefficient of the G-th tap at address 3. The taps are read out, in similar order, skipping the center tap (Tap 8), which has fixed coefficients of 1, 0, 0, 1 (i.e., the cross-tap coefficients are zero). Each tap's coefficients are read out in the I, IQ, QI, Q order.

TAP_START - Indicates the beginning of the tap readout sequence.

TAP_ENA - Indicates that the tap coefficient readout is active. This is active for four consecutive clock cycles following SYMBOL_CE.

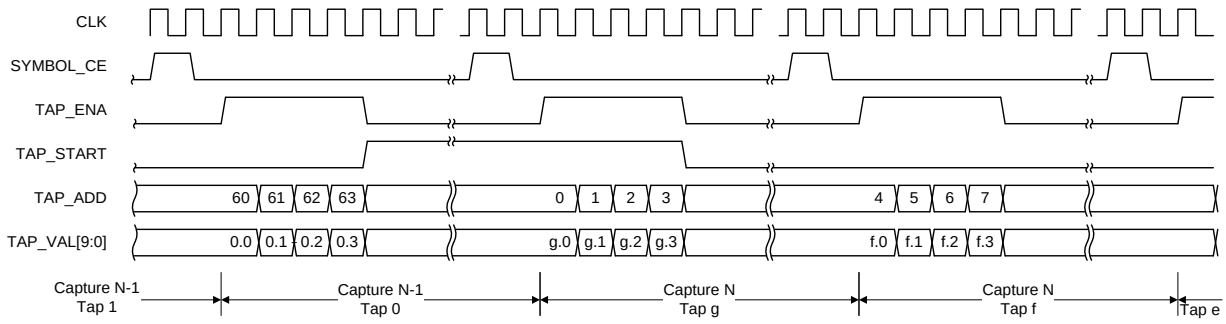

Figure 4. Timing Diagram for the Equalizer Tap Coefficient Readout. The end of the N-1th coefficient capture and beginning of the the Nth capture are shown.

AGC Control

The MPRE signal flow has a net gain of unity, with the input and output LSBs aligned. The AGC control circuits provide feedback for external circuits to maintain the desired QPSK constellation points at +/- 128 in the I and Q channels. Figure 4 shows how each AGC circuit slices the signal space to control the signal level. The feed-forward phase synchronization circuit measures the magnitude of the Equalizer output vector and asserts QCD_AGC_INCR if the Equalized signal vector is contained inside the circle shown in Fig. 4, and clears it if the vector extends outside the circle. The Slicer circuit monitors the symbol magnitude of RA_I, the I component of the phase-locked signal. If the two MSBs agree in RA_I, i.e., its magnitude is less than 128, then SLICE_AGC_INCR is asserted and it is otherwise cleared. The SLICER_AGC_GAIN and QCD_AGC_GAIN signals are the eight MSBs of twelve-bit counters that increment or decrement once each symbol depending on whether the respective X_AGC_INCR signal is asserted or not. The demanded gain is proportional to the output value, such that an input signal that is too small (as shown in Fig. 5) will result in X_AGC_GAIN increasing.

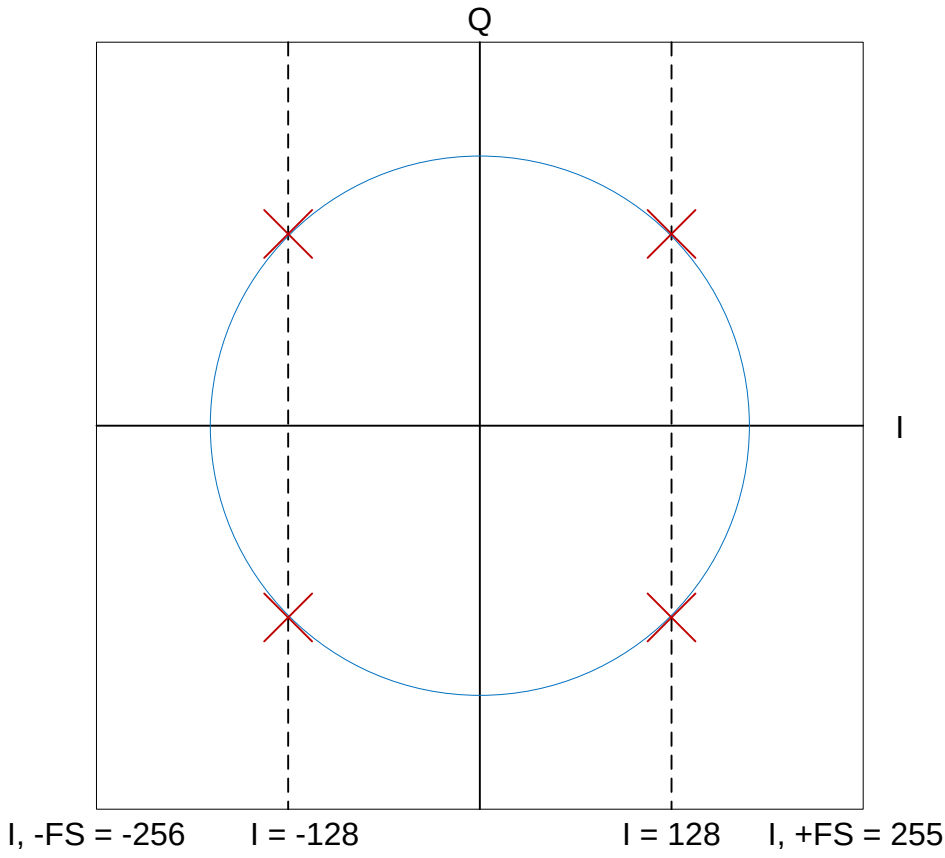

Figure 5. The AGC detectors seek to maintain the phase-locked received symbols on the red Xs. If the Equalizer output is within the blue circle the QCD_AGC_INCR signal is asserted to increase gain, and otherwise cleared to decrease gain. If the phase-locked RA_I output is between the dashed lines, SLICE_AGC_INCR is asserted to increase gain and otherwise cleared to decrease gain. The Full Scale (FS) values shown are relative to the 9-bit output signals.

Resource Utilization

The MPRE has been synthesized with the resource utilizations shown in Table 3 for the indicated Xilinx device families. Results shown are from the Xilinx XST synthesis tool with the specific devices selected as indicated.

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	FF Pairs	DSP48	RAMB36	RAMB18
Kintex-7	xc7k70t	3026	3393	1350	3939	29	10	1
Spartan-6	xc6slx75t	3026	2927	1190	3461	29	0	20
Virtex-5	xc5vlx50	3106	4341	1811	4712	29	10	1

Table 3. MPRE Resource Utilization for certain Xilinx Device Families

Input and Output Timing

The input and output timing is shown in Fig. 6 below. The output timing is consistent for all of the signal path outputs including SLICE_HD_SCALED_I/Q, SLICE_ERROR_I/Q, RA_I/Q, SD_I/Q, and EQ_I/Q.

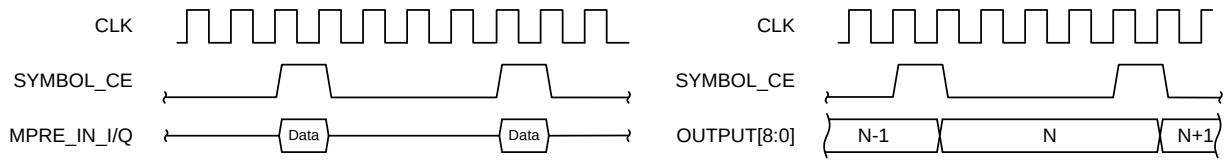

Figure 6. Timing diagrams for the signal input path (left) and output paths (right).

Ordering and Delivery

The AH1000-MPRE core is supplied as a Xilinx ngc or EDIF netlist for a user-specified Xilinx device. Each license is a permanent site license that is device-locked to the specified target device. Unlimited instantiations in the specified target device are allowed under the terms of the license. A port to or instantiation in a different device requires a new license from Anchor Hill. Each license includes six months of technical support from Anchor Hill.

Each license also includes Verilog verification test bench suites to provide a design validation and test development platform for integrators. Some test suites also include supporting C-language and/or Matlab/Octave programs to provide test stimulus files and output analysis tools.

References

[1] A. J. Viterbi and A.M. Viterbi, "Nonlinear Estimation of PSK-Modulated Carrier Phase with Application to Burst Digital Transmission," *IEEE Trans. Information Theory*, vol. IT-29 no. 4, pp. 543-551, July, 1983

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