LMS Adaptive Channel Equalizer AH1001-LEQ

ANCHORHILL COMMUNICATIONS

Product Description AH1001DS V1.0 July, 2013

INTRODUCTION

The AH1001_LEQ LMS Adaptive Channel Equalizer (LEQ) FPGA core provides a 17-tap Least Mean Squares (LMS) signed-error adaptive Channel Equalizer in a single module. The core provides automatic adaptive equalization of channel distortion and multipath effects for single-carrier communication systems.

APPLICATIONS

- Terrestrial Microwave Links
- Cellular Backhaul
- Single-Carrier Cable Transmission
- Point-to-Point or Point-to-Multipoint Systems

FEATURES

- 17-tap T-spaced complex-arithmetic LMS signed-error Channel Equalizer
- Adaptation bandwidth control (mu, step size)
- Leakage rate control (forgetting factor)
- Coefficient hold control (adaptation freeze)
- Coefficient reset control
- IQ channel and cross-tap coefficient readout
- Center taps are fixed for phase stability
- Multiplexed architecture minimizes resource utilization. Requires only 17 DSP48 blocks.
- Clock rates up to 548 MHz supported
- Symbol rates up to 1/5 of clock rate

DESCRIPTION

In wireless systems the presence of multipath reflections and various amplifier, filter, or cable distortions can cause significant degradation in the received signal resulting in poor performance or loss of signal lock. The use of an automatic channel equalizer can restore performance and substantially improve data reliability in the presence of multipath and other significant channel distortion sources.

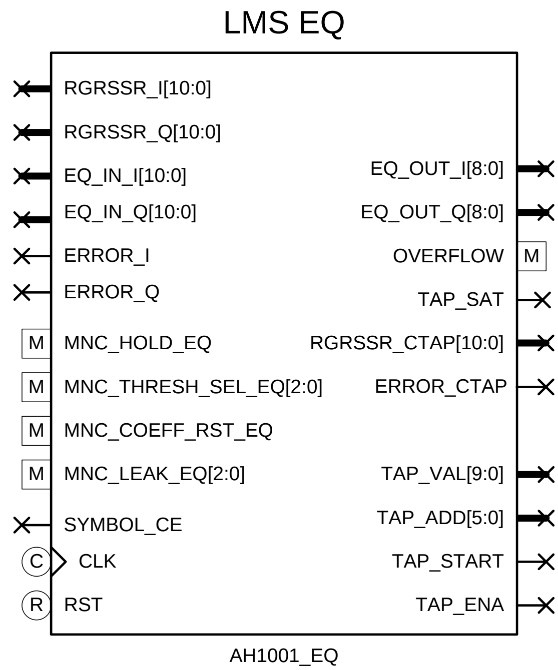

Figure 1. LMS Equalizer Schematic Symbol

The AH1001-LEQ provides an effective equalizer module for single-carrier communication signals with the automatic adaptation circuits fully integrated within the module. Other than configuration settings, the only inputs required are the signal to be equalized and the signed-error inputs generated by the slicer. The single-bit signed-error signals for the feedback path are easily generated in the slicer circuit for most modulation types, and are essentially the sign of the sliced output error. The regressor inputs are fed with a delayed copy of the input signal, as shown in Figure 2.

Using the signed-error feedback from the slicer, the equalizer applies the Least Mean Squares (LMS) algorithm to adapt the coefficients of a 17-tap linear transversal filter to equalize the effects of the propagation channel. The equalizer can effectively remove deep spectral nulls, channel tilt, multipath reflections, and other channel impairments that would otherwise cause severe performance degradation. The center tap coefficients are fixed in order to prevent interference with external phase-recovery loops.

Configuration and control inputs allow adjustment of the adaptation bandwidth (aka, mu, adaptation step size), and the coefficient leak rate (aka forgetting factor). The coefficients can also be frozen or reset with external control signals.

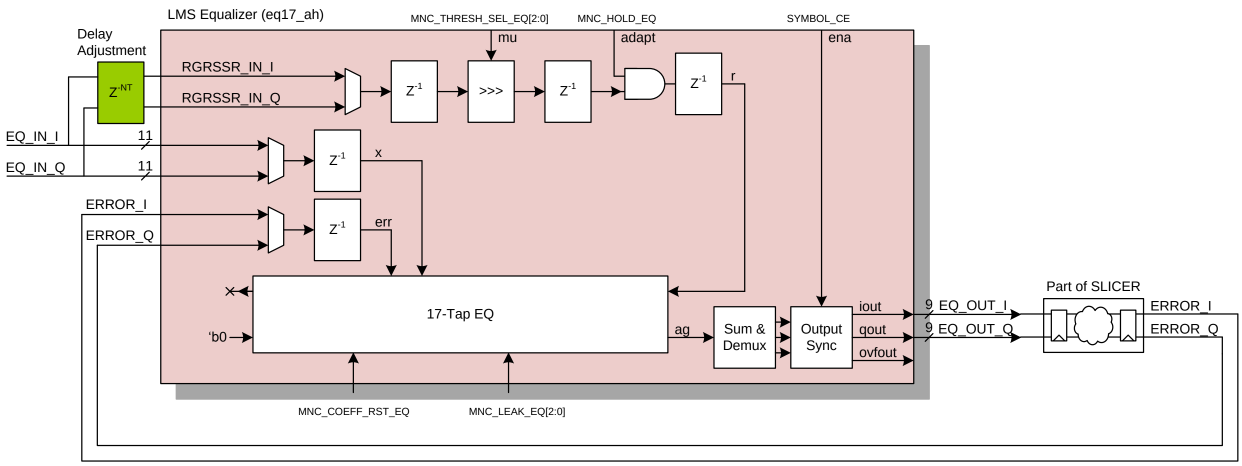

Figure 2. LMS Equalizer block diagram showing integration with a constellation slicer and the Delay Adjustment block for synchronization of the Regressor and signed-Error signals.

Resource Utilization and Speed

The LEQ 17-tap Channel Equalizer has been synthesized with the resource utilizations and speeds shown in Table 1 for the indicated Xilinx device families. Results shown are from the Xilinx XST synthesis tools with trimming disabled and the specific devices selected as indicated. Speeds shown are for -2 parts.

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	RAMB36	RAMB18	Max CLK Freq.
Kintex-7	xc7k70t	2822	1502	729	2364	17	0	0	548 MHz
Spartan-6	xc6slx75t	2831	1707	591	2091	17	0	0	140 MHz
Virtex-5	xc5vlx50t	2846	1779	813	2880	17	0	0	407 MHz
Virtex-6	xc6vlx75t	2823	1424	773	2458	17	0	0	484 MHz

Table 1. LMS Equalizer Resource Utilization and Speeds for certain Xilinx Device Families

Contact Information

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