LMS Adaptive Channel Equalizer AH1001-LEQ

Product Description AH1001DS V1.0 July, 2013

INTRODUCTION

The AH1001_LEQ LMS Adaptive Channel Equalizer (LEQ) FPGA core provides a 17-tap Least Mean Squares (LMS) signed-error adaptive Channel Equalizer in a single module. The core provides automatic adaptive equalization of channel distortion and multipath effects for single-carrier communication systems.

FEATURES

- 17-tap T-spaced complex-arithmetic LMS signed-error Channel Equalizer
- Adaptation bandwidth control (mu, step size)
- Leakage rate control (forgetting factor)
- Coefficient hold control (adaptation freeze)
- Coefficient reset control
- IQ channel and cross-tap coefficient readout
- Center taps are fixed for phase stability
- Multiplexed architecture minimizes resource utilization. Requires only 17 DSP48 blocks.
- Clock rates up to 548 MHz supported
- Symbol rates up to 1/5 of clock rate

DESCRIPTION

In wireless systems the presence of multipath reflections and various amplifier, filter, or cable distortions can cause significant degradation in the received signal resulting in poor performance or loss of signal lock. The use of an automatic channel equalizer can restore performance and substantially improve data reliability in the presence of multipath and other significant channel distortion sources.

The AH1001-LEQ provides an effective equalizer module for single-carrier communication signals with the automatic adaptation circuits fully integrated within the module. Other than configuration settings, the only inputs required

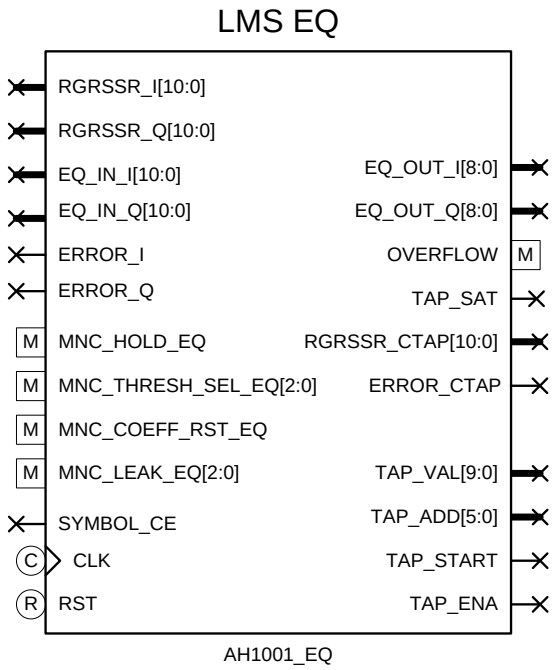

Figure 1. LMS Equalizer Schematic Symbol

are the signal to be equalized and the signed-error inputs generated by the slicer. The single-bit signed-error signals for the feedback path are easily generated in the slicer circuit for most modulation types, and are essentially the sign of the sliced output error. The regressor inputs are fed with a delayed copy of the input signal, as shown in Figure 2.

Using the signed-error feedback from the slicer, the equalizer applies the Least Mean Squares (LMS) algorithm to adapt the coefficients of a 17-tap linear transversal filter to equalize the effects of the propagation channel. The equalizer can effectively remove deep spectral nulls, channel tilt, multipath reflections, and other channel impairments that would otherwise cause severe performance degradation. The center tap coefficients are fixed in order to prevent interference with external phase-recovery loops.

Configuration and control inputs allow adjustment of the adaptation bandwidth (aka,

mu, adaptation step size), and the coefficient leak rate (aka forgetting factor). The coefficients can also be frozen or reset with external control signals.

Test points are provided to the regressor and signed-error signals at the center tap in order to allow adjustment of the external regressor delay for synchronization. The external delay in the regressor path must be adjusted to account for the delay of the signed-error signals in the user-supplied external slicer.

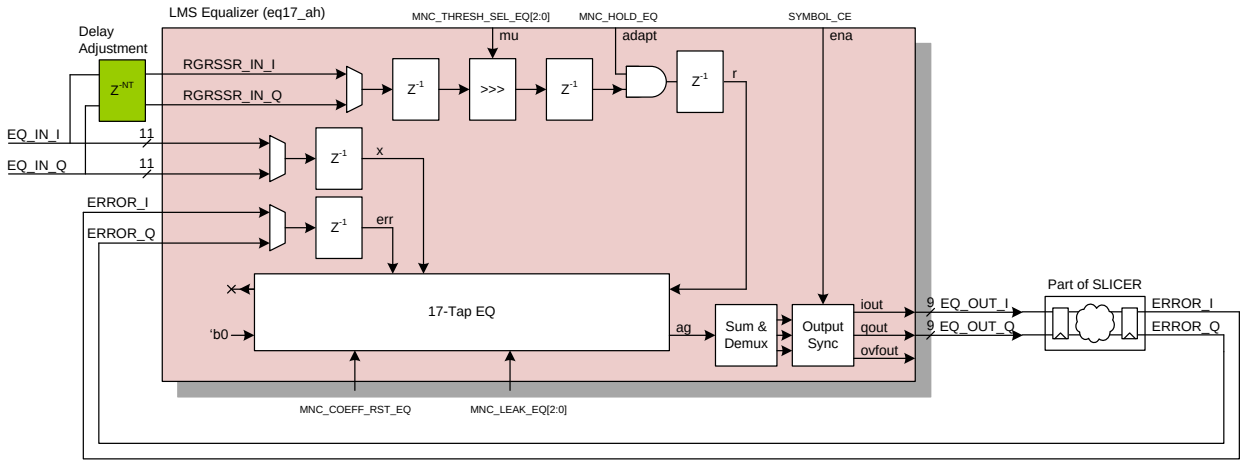

Figure 2. LMS Equalizer block diagram showing integration with a constellation slicer and the Delay Adjustment block for synchronization of the Regressor and signed-Error signals. This diagram represents the configuration used in the vfy_eq_bb.v verification testbench supplied with the LMS EQ core.

CONFIGURATION

The adaptation bandwidth control, MNC_THRESH_SEL_EQ, also called the step size (mu), or threshold select, allows selection of the adaptation rate of the LMS algorithm. Faster adaptation allows for quicker convergence, but also results in more output noise. In many applications it is beneficial to select a large adaptation bandwidth during acquisition and then reduce the setting after signal lock has been achieved.

An optional "forgetting factor", or coefficient leak rate, can be applied via the MNC_LEAK_EQ input. The coefficient leak subtracts a constant from the coefficients each symbol period.

When the leak rate is set to zero no leak occurs, and as the leak input value is incremented the leak rate increases by a factor of four. Careful use of the coefficient leak feature can help the adaptation algorithm avoid dwelling on a local minimum squared error solution when a better solution exists [1].

In addition to the adaptation bandwidth and leak rate controls, the equalizer includes coefficient hold (freeze) and reset inputs, MNC_HOLD_EQ and MNC_COEFF_RST_REQ, respectively. Each control affects only the equalizer coefficients and not the control logic.

SIGNAL DESCRIPTIONS

Signal	Direction	Description
RGRSSR_I/Q[10:0]	Input bus	Baseband signal input
EQ_IN_I/Q[10:0]	Input bus	Baseband signal input
ERROR_I/Q	Input	Signed-error inputs from slicer
SYMBOL_CE	Input	Symbol input clock enable
CLK	Input	System clock input
RST	Input	Module reset
MNC_HOLD_EQ	Input	Equalizer coefficient hold
MNC_THRESH_EQ_SEL[2:0]	Input bus	Equalizer adaptation bandwidth (mu)
MNC_COEFF_RST_EQ	Input	Equalizer coefficient reset
MNC_LEAK_EQ[2:0]	Input bus	Equalizer coefficient leak rate (0 = no leak)
EQ_OUT_I/Q[8:0]	Output bus	Equalizer output
RGRSSR_CTAP[10:0]	Output bus	Regressor value at center tap (test point)
ERROR_CTAP	Output	Signed-error value at center tap (test point)
OVERFLOW	Output	Active if arithmetic overflow in any Equalizer tap
TAP_SAT	Output	Active if any Equalizer tap coefficient reaches max value
TAP_VAL[9:0]	Output bus	Equalizer tap debug coefficient value readout
TAP_ADD[5:0]	Output bus	Equalizer tap debug coefficient address readout
TAP_START	Output	Equalizer tap debug readout cycle start indicator
TAP_ENA	Output	Equalizer tap debug readout output enable

Table 1. LMS Equalizer Input and Output Signal Descriptions

Inputs

RGRSSR_I/Q[10:0] - These are the LMS Equalizer regressor inputs. These are the EQ_IN_I and EQ_IN_Q baseband, time-synchronized, symbol inputs represented in two's complement, potentially delayed external to the equalizer depending on external processing latencies. The default input width is eleven bits but is parameterized. See the *Regressor and Signed-Error Timing Synchronization* section below regarding synchronization of this signal.

EQ_IN_I/Q[10:0] - These are the I and Q baseband, time-synchronized, symbol inputs represented in two's complement. The default input width is eleven bits but is parameterized.

ERROR_I/Q - The signed-error inputs. This the sign bit of the two's complement sliced error vector or the vector difference between the ideal estimated received constellation and the received symbol vector. These inputs may need to be delayed externally for synchronization depending on external processing latencies. See the *Regressor and Signed-Error Timing Synchronization* section below regarding synchronization of this signal.

SYMBOL_CE - This is the input clock enable for the input signals. When SYMBOL_CE is asserted (high) the **EQ_IN_I/Q**, **RGRSSR_IN_I/Q**, and **ERROR_I/Q** inputs are clocked in at the rising edge of CLK. SYMBOL_CE should not be asserted longer than one period of CLK and should remain inactive for at least four clock periods after assertion. The output signals are also updated when SYMBOL_CE is active.

CLK - System clock input.

RST - Reset. The internal logic is forced to an initialization state when asserted. All coefficients and control logic are reset by this signal.

MNC_HOLD_EQ - When asserted (high) the equalizer stops adapting and freezes the tap coefficients.

MNC_THRESH_EQ_SEL[2:0] - This three-bit value controls the adaptation bandwidth, or step size, (mu) of the Equalizer adaptation. Eight discrete power-of-two selections are used, such that larger values result in wider adaptation bandwidth, which scales with the symbol rate, Rs.

000 : 4.4545e-05 * Rs (narrowest adaptation BW)
001 : 8.5580e-05 * Rs
010 : 1.7132e-04 * Rs
011 : 3.4941e-04 * Rs
100 : 6.9735e-04 * Rs
101 : 1.3889e-03 * Rs
110 : 2.7548e-03 * Rs
111 : 6.2893e-03 * Rs (widest adaptation BW)

MNC_COEFF_RST_EQ - Equalizer Coefficient Reset. When asserted (high) the Equalizer coefficients are set to zero.

MNC_LEAK_EQ[2:0] - Equalizer tap coefficient leakage control. Coefficients will slowly decay to zero in the absence of significant error feedback when this feature is enabled. Set MNC_LEAK_EQ = 0 to disable coefficient leakage. The leak rate increases by 4x for each increment towards maximum.

Outputs

EQ_OUT_I/Q[8:0] - Two's complement Equalizer output.

EQ_OVERFLOW - Arithmetic overflow indicator for the Equalizer outputs. The EQ_OUT_I/Q outputs are processed by a Clip-and-Round stage when taken from the tap accumulators. If the output is saturated EQ_OVERFLOW is set until the next output symbol.

TAP_SAT - Saturation indicator for the Equalizer coefficients. If any coefficient reaches its maximum or minimum value this signal will assert until the condition clears.

RGRSSR_CTAP[10:0] - This unregistered test point is the multiplexed, delayed **RGRSSR_I/Q** input at the Equalizer center tap. See the *Regressor and Signed-Error Timing Synchronization* section below regarding the use of this signal for synchronization of **RGRSSR_I/Q** and **ERROR_I/Q** input signals. Once synchronization has been verified it is recommended to leave this signal unconnected.

ERROR_CTAP - This unregistered test point is the multiplexed signed-error **ERROR_I/Q** input at the Equalizer center tap. See the *Regressor and Signed-Error Timing Synchronization* section below

regarding the use of this signal for synchronization of **RGRSSR_I/Q** and **ERROR_I/Q** input signals. Once synchronization has been verified it is recommended to leave this signal unconnected.

TAP_VAL[9:0] - Two's complement Equalizer tap coefficient values, automatically read out as the equalizer processes symbols. See Figure 3 for output timing details.

TAP_ADD[5:0] - The address of the tap coefficient currently being read out. The address starts at 0 for the I-channel coefficient of Tap G (the 17th tap), followed by the I-to-Q cross tap at address 1, the Q-to-I cross tap at address 2, and the Q-channel coefficient of the G-th tap at address 3. The taps are read out, in similar order, skipping the center tap (Tap 8), which has fixed coefficients of 1, 0, 0, 1 (i.e., the cross-tap coefficients are zero). Each tap's coefficients are read out in the I, IQ, QI, Q order. See Fig. 3.

TAP_START - Indicates the beginning of the tap readout sequence.

TAP_ENA - Indicates that the tap coefficient readout is active. This is active for four consecutive clock cycles following SYMBOL_CE.

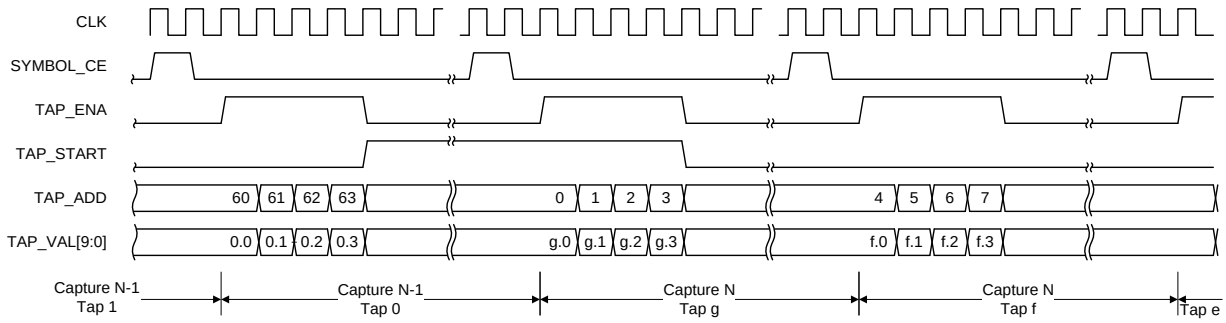

Figure 3. Timing Diagram for the Equalizer Tap Coefficient Readout. The end of the N-1th coefficient capture and beginning of the the Nth capture are shown.

Resource Utilization and Speed

The LEQ 17-tap Channel Equalizer has been synthesized with the resource utilizations and speeds shown in Table 2 for the indicated Xilinx device families. Results shown are from the Xilinx XST synthesis tools with trimming disabled and the specific devices selected as indicated. Speeds shown are for -2 parts.

Family	Device	Slice Regs	Slice LUTs	Occupied Slices	LUT-FF Pairs	DSP48	RAMB36	RAMB18	Max CLK Freq.
Kintex-7	xc7k70t	2822	1502	729	2364	17	0	0	548 MHz
Spartan-6	xc6slx75t	2831	1707	591	2091	17	0	0	140 MHz
Virtex-5	xc5vlx50t	2846	1779	813	2880	17	0	0	407 MHz
Virtex-6	xc6vlx75t	2823	1424	773	2458	17	0	0	484 MHz

Table 2. LMS Equalizer Resource Utilization and Speeds for certain Xilinx Device Families

Input and Output Timing

The input and output timing is shown in Fig. 4 below. The input timing is consistent for all of the input signal paths, EQ_IN_I/Q, RGRSSR_I/Q, and ERROR_I/Q.

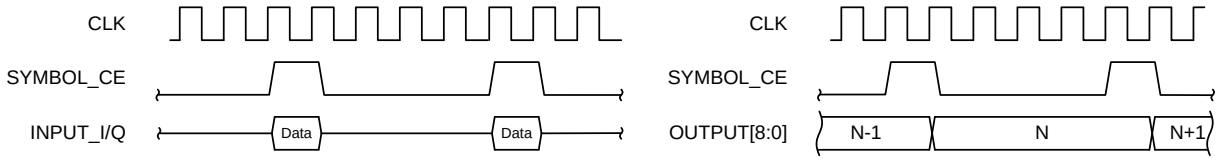

Figure 4. Timing diagrams for the signal input path (left) and output paths (right).

Regressor and Signed-Error Timing Synchronization

In order for the LMS algorithm to converge the signed-error value associated with a particular input sample in the regressor stream must reach the equalizer center tap at the same symbol time as the associated regressor sample. Since the regressor path propagates through the equalizer taps in the reverse direction of the data and the signed-error input is presented to all taps at once, it is crucial for the convergence of the LMS algorithm that the correct regressor and signed-error samples arrive at the center tap at the proper time. The arrival time of the signed-error signals at the equalizer input are dependent on the latency of the equalizer output signal through the external slicer and any other signal processing between the equalizer and the slicer that may be implemented.

Typically the external delays in the signed-error signal are handled by adding a compensating delay buffer between the EQ_IN_I/Q equalizer input signals and the RGRSSR_I/Q regressor inputs as shown in Figure 2 above. In order to properly adjust the appropriate delay value, the RGRSSR_CTAP and ERROR_CTAP test points are provided. When used with a test signal composed of a single non-zero symbol value in a stream of zeros, the regressed input and signed-error can be easily aligned at the center tap using the RGRSSR_CTAP and ERROR_CTAP test points.

Figure 5 shows an example of the proper signal timing using the impulse test input signals generated in the vfy_eq_bb.v Verilog verification testbench supplied with the LMS EQ core. Substituting the chan_i/q signals for the file_in_i/q signals in the testbench by commenting out the file_in_i/q input signals and uncommenting the chan_i/q signals in both the delay buffer and the Equalizer instantiations enables delay adjustment for synchronization.

As shown in Fig. 5, when synchronization is correct the regressor and signed-error signal alignment at the center tap are readily apparent when the test signal is used. The example slicer used in the vfy_eq_bb.v testbench requires a compensating delay of five symbols (two for the slicer and three for the output latency in the equalizer), which can be seen in the delay from the impulse in the chan_i signal to the rgrs_dly_i signal in Fig. 5. Two symbols after the impulse appears at the output of the equalizer in the eq_out_i signal the sliced signed-error for the impulse appears at the center tap as shown by err_ctap, which is connected to the ERROR_CTAP output port. The I-channel of the delayed RGRSSR_I/Q

signal appears at the center tap as rgrsr_ctap, which is connected to the RGRSSR_CTAP output port, at the same symbol time (as indicated by the SYMBOL_CE pulse). This indicates that the correct delay has been applied and the ERROR_I/Q and RGRSSR_I/Q signals are properly synchronized.

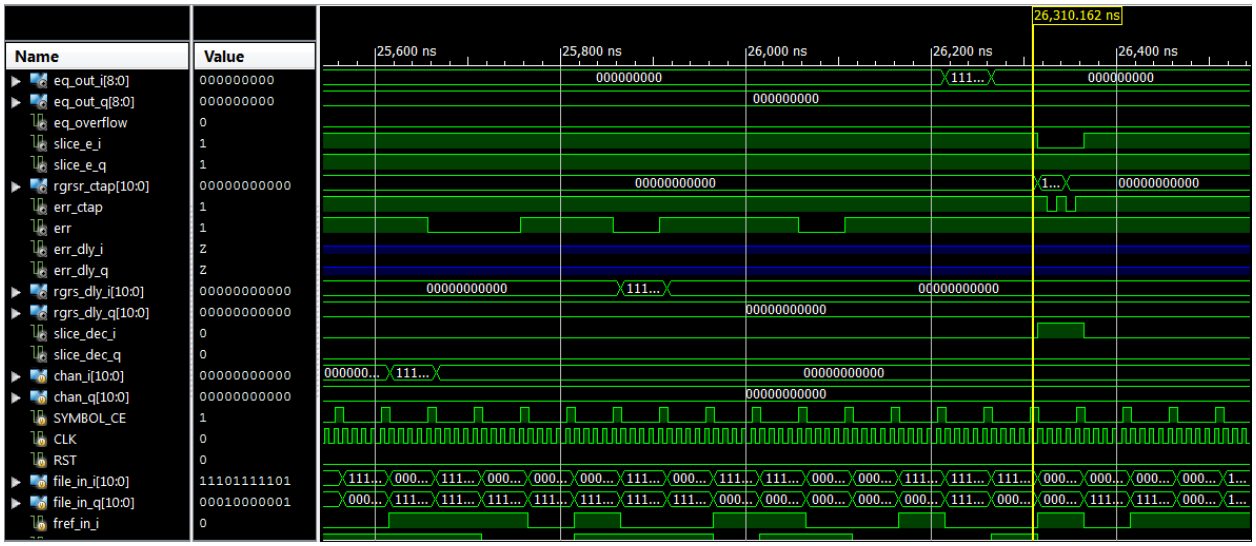

Figure 5. Timing diagram of the adjustment of the RGRSSR_I/Q delay shown by the RGRSSR_CTAP (rgrsr_ctap) and ERROR_CTAP (err_ctap) outputs. The input pulse at the chan_i input appears in both signals at the center tap at the same symbol time (marker).

Note that the RGRSSR_CTAP and ERROR_CTAP signals contain both the I and Q channel inputs multiplexed together. Since the delays in the I and Q channels are identical a distinct impulse in either channel that causes a change in the corresponding ERROR_I/Q signal can be used for synchronization.

Ordering and Delivery

The AH1001-LEQ core is supplied as a Xilinx ngc or EDIF netlist for a user-specified Xilinx device. Each license is a permanent site license that is device-locked to the specified target device. Unlimited instantiations in the specified target device are allowed under the terms of the license. A port to or instantiation in a different device requires a new license from Anchor Hill. Each license includes six months of technical support from Anchor Hill.

Each license also includes Verilog verification test bench suites to provide a design validation and test development platform for integrators. Some test suites also include supporting C-language and/or Matlab/Octave programs to provide test stimulus files and output analysis tools. The AH1001-LEQ Equalizer also includes Verilog source code to instantiate Xilinx SRL elements for the external adjustable-delay block required for configuring the core to the user's application, as well as an example QPSK slicer for generation of the signed-error signals.

Certain customizations, such as changing the number of taps or the input or output precision, are available. Contact Anchor Hill Communications for more information.

References

[1] Bernard Widrow, Samuel D. Stearns: *Adaptive Signal Processing*, Prentice Hall, 1985, ISBN 0-13-004029-0

Important Stuff

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